ABSTRACT

A semiconductor integrated circuit including a plurality of ADCs subjected to interleave-operation in parallel, or a semiconductor integrated circuit including an imaging ADC using a plurality of circuit elements to be switched sequentially, in which even when an image signal of any specification is input, an output signal of the plurality of ADCs or the imaging ADC is averaged to reduce irregularities on a screen. The semiconductor integrated circuit includes a plurality of analog/digital converting circuits (11) operated in parallel for sequentially converting an analog image signal to a digital image signal, a multi-phase clock signal generating circuit (12) for generating multi-phase clock signals to be used for periodically operating the plurality of analog/digital converting circuits (11) in a certain order, and a control circuit (20) for controlling the multi-phase clock signal generating circuit (12) to change a period or an order of operating the plurality of analog/digital converting circuits (11).